REMARKS

Claims 31 and 37 have been amended. Claim 34 has been canceled.

The Examiner has rejected applicants' claims 31-37 under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most clearly connected, to make and/or use the invention. In particular, the Examiner has stated that the "specification does not describe a converter for converting third parallel data of M bits into fourth parallel data of N bits, the third parallel data being derived from first parallel data of N bits received by an input unit as specified in claims 31 and 37." The Examiner has further stated that the "specification does not describe an error correction unit that error corrects second parallel data of N bits received by the input unit as specified in claims 31 and 37." This rejection is respectfully traversed.

Applicants submit that the specification does describe the above-mentioned converter and error correction unit of applicants' claims. In particular, the converter buffer 16 of the apparatus shown in FIG. 2 of applicant's drawings serves to change the third parallel data of 4 bits at its input to fourth parallel data of 8 bits at its output, where the third parallel data, in turn, was delivered from the output of the compressor 14 which generated the data from the first parallel data of 8 bits supplied to the input of the compressor. The error correction units, ECC Encoders 54-1-54-3, furthermore, selectively provide error correction check code data to the aforementioned fourth parallel data of 8 bits delivered to a first terminal of the switch 18 and to the second parallel data of 8 bits delivered to a second terminal of the switch.

Applicants' specification, therefore, contains a description which is sufficient to enable a skilled artisan to make and use applicants' invention. In particular, the specification provides an adequate description of the converter and the error correction unit. Applicants' claims 31-37 are thus supported by an enabling disclosure and, hence, are in compliance with the provisions of 35 USC § 112, second paragraph.

The Examiner has further rejected applicants' claims 31-37 under 35 USC § 103(a) as unpatentable over the Yoshimura, et al. patent taken in view of Official Notice. With respect to applicants' claims, as amended, this rejection is respectfully traversed.

Applicants' independent claims 31 and 37 are directed to a digital information coding apparatus and method in which an input unit selectively inputs first and second parallel data of N bits representing first and second digital information of different bit rates. An encoder encodes the first parallel data to generate third parallel data of M bits, where $M \neq N$. A converter converts the third parallel data into fourth parallel data of N bits. An error correction unit selectively adds an error correction check code to the second parallel data and the fourth parallel data. The latter unit performs common addition processing irrespectively of the second parallel data and the fourth parallel data.

Such a construction is not taught or suggested by the cited art of record. In particular, the Yoshimura, et al. patent teaches " an apparatus ... in which the number of data in an audio synchronizing block containing audio data and synchronizing data is selected ...to be equal to that of data in a video synchronizing block containing video data and synchronizing data... ." The Yoshimura, et al. patent utilizes encoding means and error correction means to generate the

synchronization blocks and, in particular, the Examiner has pointed to FIGS. 5 and 7 of the Yoshimura, et al. patent as illustrative of the system of the patent. While FIGS. 5 and 7 of the patent show inputting video and audio data and converting this data to digital data, there is nothing taught in the patent that these signals are each the same bit data, i.e., N bit data. This does not appear to be taught in column 5, lines 5-45 of the Yoshimura, et al. patent cited by the Examiner.

Also, there is nothing taught or suggested in the patent of encoding one of these parallel data to third parallel data of a different number of bits, i.e., M bits, and then converting the M bit data into fourth parallel data of N bits. The passages and figures of the patent cited by the Examiner, i.e., column, 5, lines 5-45, column 3, lines 12-65, and FIGS. 10-11, and the elements cited by the Examiner, 104, 108, 110, 111, and 112, clearly are not taught to perform this type of operation. Moreover, even if the compression circuit 12 in FIG. 5 changed the bit number of the input video data, there is no converter to change that bit number back to the original bit number, i.e., no conversion from N bits to M bits and then back to N bits.

Moreover, in the video and audio synchronization blocks shown in FIGS. 10 and 11 of the Yoshimura, et al. patent, there are different amounts of error correction code in each block. Therefore, there is no common addition processing irrespective of the type of parallel data. Finally, the unit 30 in the patent is a synchronization adding circuit and does not convert a parallel signal to a different bit signal.

Based on all of the above, the Yoshimura, et al. patent does not teach or suggest the features of applicants' independent claims 31 and 37, i. e., does not teach or suggest an

apparatus and method comprising the following features: selectively inputting a first parallel data of N bits representing a first digital information and second parallel data N bits representing a second digital information, wherein a bit rate of the first digital information differs from a bit rate of the second digital information, encoding the first parallel data to generate third parallel data of M bits ($M \neq N$), converting the third parallel data into fourth parallel data of N bits, and selectively adding an error correction check code to the second parallel data and/ or the fourth parallel data, and said adding performing a common addition processing irrespectively of the second parallel data and the fourth parallel data.

In view of the above, it is submitted that applicants' claims, as amended, patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is respectfully requested.

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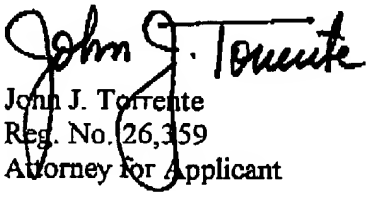
Respectfully submitted,



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Version With Markings To Show Changes Made

IN THE CLAIMS

Amend claim 31 as follows:

-- 31. (Amended) A digital information coding apparatus, comprising:

a) an input unit, arranged to selectively [inputting] input a first parallel data of N bits representing a first digital information and second parallel data of N bits representing a second digital information, wherein a bit rate of the first digital information differs from a bit rate of the second digital information;

b) an encoder, arranged to encode the first parallel data to generate third parallel data of M bits ($M \neq N$);

c) a converter, arranged to convert the third parallel data into fourth parallel data of N bits; and

d) an error correction unit, arranged to selectively add an error correction check code to the second parallel data and the fourth parallel data,

said error correction unit performing a common addition processing irrespectively of second parallel data and the fourth parallel data. –

Cancel claim 34.

Amend claim 37.

-- 37. (Amended) A digital information coding method, comprising:

selectively inputting a first parallel data of N bits representing a first digital information and second parallel data N bits representing a second digital information, wherein a bit rate of

the first digital information differs from a bit rate of the second digital information;

encoding the first parallel data to generate third parallel data of M bits ($M \neq N$);

converting the third parallel data [to] into fourth parallel data of N bits; and

selectively adding [an] a predetermined data amount of error correction check code for every predetermined data amount of to the second parallel data [and] or the fourth parallel data,

said adding step performing a common addition processing irrespectively of the second parallel data and the fourth parallel data. --.